REMARKS

Claims 1, 3, 5-7, 11-17 and 20-22 are pending in the application.

Claims 1, 3, 5-7, 11-17 and 20-22 had been rejected.

Claims 1, 2, 4, 8-10, 18 and 19 have been cancelled without prejudice.

Claims 3, 5-7, 11, 13, 15-17 and 20-22 have been amended, as indicated above.

New Claim 23 is presented to substitute for rejected Claim 1.

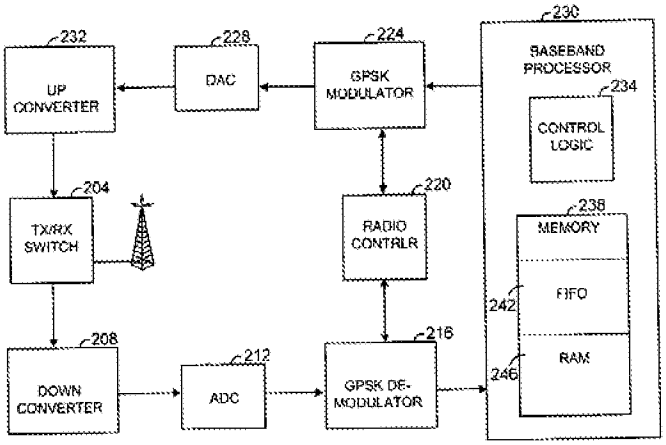
No new matter has been added.

Reconsideration of the Claims is respectfully requested.

1. New Ground of Rejection under Section 112, second paragraph

Per the decision of June 1, 2010, the BPAI had "*pro forma* reversed the two outstanding rejections under 35 U.S.C. § 103 that encompass all claims on appeal, claims 1, 3, 5 through 7, 11 thorugh 17, and 20 through 22. [The BPAI has] instituted [their] own rejection of all these claims on appeal under 35 U.S.C. § 112, second paragraph." (BPAI Decision at p. 6).

With respect to Applicant's Independent Claim 1, the Board states that "the variously recited circuit elements are not stated to cooperate with each other, let alone with the label-described recitations at the end of this claim." New Claim 23 is presented to substitute for Independent Claim 1, which has been cancelled without prejudice, and reflects cooperation among the elements as supported by Applicant's Specification and Figures. (*see* Specification at pp. 12-14; Figure 2):



Applicant respectfully submits that new Claim 23, and Claims 3, 5 and 6 that depend from Claim 23, overcome this rejection.

With respect to Applicant's Claim 7, the Board states that "the body of this claim does not recite any transmission of data as set forth in the preamble of this claim." (Board Decision at p. 5). As reflected in Applicant's Specification, the method relates to a "method for storing and accessing data that is to be transmitted thorugh a radio modem . . . ." (Specification at p. 14, *ll.* 18-20). Applicant's Claim 7 has been amended to reflect "accessing" as supported by Applicant's Specification, and further to reflect implementation via baseband processing circuitry, and relation to transmission by a wireless communication device. Applicant respectfully submits that amended Claim 7, and Claims 11-16 that depend from Claim 7, overcome this rejection.

With respect to Applicant's Claim 17, the Board states that "[i]ndependent claim 17 recites in its preamble a baseband processing system to which he body of this claim does not refer." (Board Decision at p. 5). Applicant has amended Claim 17 to recite a memory structure formed with a baseband processing circuitry, as supported by the Specification, and further recites the definition of the memory portions with the baseband processing circuitry set out by the preamble. Further amendments have been presented to further clarify the purpose of the elements within the claims. Also, dependent claim 22 has been amended to replace "related to" with "corresponds to," as supported by Applicant's Specification. (*See* Specification at p. 24, *ll.* 20-22). Applicant respectfully submits that amended Claim 17, and amended Claims 20-22 that depend from Claim 17, overcome this rejection.

Applicant respectfully submits that the amended claims, tendered in conformity with the Board's statement, overcome the new grounds of rejection submitted by the Board under Rule 41.50(b).

2. Rejection under 35 USC § 103

In the Final Office Action, Claims 1, 3, 5-7, 11-17, 20 and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over US Published Application 2002/0183013 to Auckland et al ("Auckland"), in view of US Patent No. 5,968,143 to Chisholm et al ("Chisholm"), and further in view of U.S. Patent No. 6,434,630 to Micalizzi Jr, et al ("Micalizzi").

The BPAI submits that its "decision in this regard is based solely on the indefiniteness of the claims subject matter and does not reflect the adequacy or the inadequacy of the prior art evidence supplied in support of the rejection before [it]." (BPAI Decision at p. 4).

In this regard, the Applicant resubmits its position in response to the Final Office Action of April 13, 2007, ("Final Office Action"), with respect to the claims as amended.

Applicant respectfully submits that a *prima facie* showing of obviousness has not been shown by the hypothetical combination of the front-end controller of Aukland, in view of the command block transfer over an expansion bus of Chisholm, and the I/O completion interrupt minimization of Micalizzi, because the hypothetical combination does not provide a suggestion or motivation, either alone or in combination, in achieving Applicant's invention as defined by its claims, nor does the hypothetical combination teach or suggest the limitations as set out by Applicant's claims.

Auckland relates to an "analog RF hardware in the front ends of personal and mobile communication radios that is reconfigurable for a variety of air interface standards." (Auckland ¶ 0048). In this regard, Auckland generally recites *memory in an operational usage* for RF portion 600 configurations, which includes a "controller 614 may be dedicated to controlling the RF front end of the radio, including functions such as modulation, demodulation, encoding and decoding. In a software definable radio, where the radio hardware is fixed but may be customized by on-board *software during operation to allow the radio to operate in conjunction with a particular air interface standard or on a particular frequency band, the customization operation may be controlled by the controller 614.*" (Auckland ¶¶ 0077, 0090; *see* Figure 6) (emphasis added).

The Office Action mailed January 23, 2006, noted that "Auckland does not describe the memory structure for storing addresses for accessing data blocks." (Office Action mailed

January 23, 2006 at p. 7). Further, Auckland pays passing, if any, attention to data access. Instead, Auckland recites antenna configuration techniques (see, e.g., Auckland Claim 1), and radio configuration techniques (*see, e.g.*, Auckland Claim 15; *cf.* Auckland ¶ 0143 ("Other components of the radio may access data in the memory over a system bus or other communication means."). Accordingly, Applicant respectfully submits that Auckland does not teach or disclose memory data access.

Chisholm relates to "transfer of command blocks between two processing units communicating over an expansion bus." (Chisholm 1:16-17). In this regard, Chisholm's Summary of the Invention recites a "*command block transfer controller* [that] is *responsive to the transfer start signal* written by the host processing unit to start a command transfer for retrieving a command block from a corresponding host memory portion without local processing unit intervention." (Chisholm 3:1-4) (emphasis added).

But the device of Chisholm relates to command block transfer, not data transfer, to local processing sides within a personal computer. For example, Chisholm recites that "[during] a *command block transfer* from the host processing side 110 to the local processing side 120, the FIFO buffer 326 receives and temporarily stores the *command block* from the host DMA state machine 322 and provides such *temporarily stored command block* to the local DMA state machine 324 to be stored in a *command block portion* of the local memory." (Chisholm 5:16-22).

Further, the command block of Chisholm "includes a command portion and a command address portion appended thereto." (Chisholm Claim 2). The "command address portion includes a chain enable information indicating whether another command block is chained to the transferred command block." That is, Chisholm *does not address* data transfer. Further, the dissimilar command blocks of Chisholm do not include addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use.

Micalizzi relates "to a host adapter which reduces the number of input/output (I/O) completion interrupts generated from the host adapter to a host microprocessor." (Micalizzi 1:9-12). That is, Micalizzi is a device to increase processor performance by "combining successful

I/O completion reports and reducing the number of interrupts, the host adapter reduces the overhead incurred in servicing interrupts for successfully completed I/O requests. This reduces the amount of processing time (`I/O bound` time) and power spent by the host microprocessor in *processing interrupts from the adapter*, and creates more time and power for the host microprocessor to *process user applications*. In one embodiment of the present invention, the amount of time and/or resources (e.g., power) spent by the host microprocessor in servicing interrupts (CPU utilization) is decreased by 20%." (Micalizzi 2:5-15). Micalizzi does not address command blocks with addresses of data blocks and indicators for command blocks.

In contrast to the hypothetical combination cited by the Final Office Action, Applicant's New Independent Claim 23 recites, *inter alia*, a "*wireless transceiver device,* comprising: a transmit/receive switch to selectively transmit radio frequency signals and to receive radio frequency signals; transmission circuitry to receive digital data and to convert the digital data to radio frequency signals for transmission . . . ; receiver circuitry coupled to receive radio frequency signals from the transmit/receive switch . . . ; and baseband processing circuitry coupled to provide the digital signals to the transmission circuitry and to receive the demodulated digital signals from the receiver circuitry, the baseband processing circuitry including: a first in, first out (FIFO) memory structure for storing addresses for accessing data blocks to order the digital data to provide the transmitter circuitry; and a plurality of command blocks formed within another memory structure, and a portion of the another memory structure that stores an indicator that indicates whether a command block of the plurality of command blocks is in use, wherein each of the command blocks includes addresses of data blocks stored within the another memory structure."

Applicant's Independent Claim 7 as amended recites, *inter alia*, a "method for storing and retrieving data in a baseband processing circuitry for transmission by a wireless communication device, comprising: storing a data block in random access memory of the baseband processing circuitry; and storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure of the baseband processing circuitry, the pointer includes an address of a command block; storing an address of the data block in the command block; and setting an indicator signal in a defined memory location, wherein the indicator signal indicates

that the data block address stored in the command block is for data that has yet to be successfully transmitted and that the command block is busy." (emphasis added).

Also, Applicant's Independent 17 as amended recites, *inter alia*, a "memory structure formed within a baseband processing circuitry, comprising: a random access memory portion defined within the baseband processing circuitry to store data blocks that are to be transmitted via a radio modem in a first in, first out (FIFO) order; a FIFO memory structure defined within the baseband processing circuitry to store pointers that correspond to the data blocks stored in the random access memory portion; a plurality of command blocks further defined within the random access memory portion, wherein each of the command blocks specifies an address of a data block that is to be transmitted; and a defined memory portion that stores command block indicators for each command block, wherein each of the command block indicators specify whether its corresponding command block includes the address of a data block that has yet to be successfully transmitted via the radio modem."

Applicant respectfully submits that a *prima facie* case of obviousness has not been set out. There is no suggestion or motivation to modify the reconfigurable RF front end of Auckland with the command block transfer of Chisholm, and further with the interrupt reduction of Micalizzi to achieve Applicant's claimed invention. Further, the cited references do not teach or suggest all the limitations of Applicant's claimed invention.

Applicant respectfully requests that the rejection to New Independent Claim 23 and Claims 2, 5, and 6 that depend therefrom, to amended Independent Claim 7 and Claims 11-16 that depend directly or indirectly therefrom, and to amended Independent Claim 17 and Claims 20-22 that depend directly or indirectly therefrom, be withdrawn.

3. Conclusion

As a result of the foregoing, the Applicant respectfully submits that Claims 3, 5-7, 11-17, and 21-23 in the Application are in condition for allowance, and respectfully requests allowance of such Claims.

No additional fees are believed to be due. In the event that additional fees are due or a credit for an overpayment is due, the Commissioner is hereby authorized to charge any

additional fees or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126.

The Examiner is invited to contact the undersigned by telephone, facsimile, or email if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,
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